Remarks

The Office Action mailed December 4, 2002 has been received and the Examiner's comments carefully reviewed. The specification has been amended to correct minor typographical errors. Claims 1-20 were pending prior to entry of this Amendment. Claims 13-20 are allowed. Claims 1 and 7 have been amended. Claim 8 has been cancelled. No new subject matter has been added. Claims 1-7 and 9-20 are currently pending, with Claims 13-20 allowed. Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."** For at least the following reasons, Applicant respectfully submits that the pending claims are in condition for allowance.

Allowable Subject Matter

Claim 8 was objected as being dependent on a rejected base claim, but allowable if written in independent form including all of the limitations of the base claim and any intervening claims. In particular, the Examiner indicated that "an integrated video wherein the pixel frequency is based on an external clock reference and wherein the re-clocking circuit is based on the external clock reference" recites allowable subject matter. Claim 7 has been amended to include the salient limitations of Claim 8. Accordingly, Claim 7 is proposed to be allowable, and each of Claims 9-12 are allowable at least because they depend on allowable Claim 7.

Rejection of Claims 1-7 and 9-11 under 35 U.S.C. § 102(e)

Claim 1 was rejected under 35 U.S.C. § 102(e) as being unpatentable in view of Ishii et al. (US 2002/0036723). Claim 1 was amended to further recite the allowable subject matter identified by the Examiner in Claim 8. In particular, Claim 1 is allowable at least because the prior art of record does not disclose "providing a local clock signal to re-clock the video data signal between the video data signal circuitry and output circuitry, the local clock signal being based on the external clock reference" as recited in Applicant's Claim 1. Accordingly, it is respectfully submitted that Claim 1, as amended, is allowable and notice to that effect is earnestly solicited. Claims 2-6 are allowable at least because they depend from Claim 1.

Claim 7 was rejected under 35 U.S.C. § 102(e) as being unpatentable in view of Ishii et al. (US 2002/0036723). As noted above, Claim 7 was amended to include the salient limitations

of Claim 8. For this reason, it is respectfully submitted that Claim 7 is allowable, and notice to that effect is earnestly solicited. Claims 9-12 are allowable because they depend from Claim 7, which is proposed to be allowable.

Summary

It is respectfully submitted that each of the presently rejected claims (Claims 1-7 and 9-12) are in condition for allowance and notification to that effect is requested. The Examiner is invited to contact Applicant's representative at the below-listed telephone number if it is believed that prosecution of this application may be assisted thereby. Although certain arguments regarding patentability are set forth herein, there may be other arguments and reasons why the claimed invention is patentably distinct. Applicant reserves the right to raise these arguments in the future.

MERCHANT & GOULD P.C.
P.O. Box 2903, Minneapolis, MN 55402-0903
206.342.6200

By: _____
Name: John E. Whitaker
Reg. No.: 42,222
Direct Dial: 206.342.6256

Version With Markings To Show Changes Made

In the Specification:

The paragraph beginning at line 10 of page 6 has been amended as follows:

(Amended) The first operation mode (Scheme A) occurs when the scheme select switch 123 is in the "A" position. In that position, the processed pixel clock signal 11[1]7 is coupled to a first D flip-flop 125, a second D flip-flop 127, and to the RGB DAC 129. It will be appreciated that although only a single flip-flop and DAC may be shown in FIGURE 1, there may in fact be several D flip-flops and DACs, one per data line. In this configuration, the processed pixel clock 117 is used to latch the video data signal 121 through to the RGB DAC 129.

The paragraph beginning at line 23 of page 7 has been amended as follows:

(Amended) The clock phase selector 131 selects the proper clock phase for its two clock outputs so that the appropriate flip-flops (12[5]7 and 133) operate with proper setup and hold times. There are several options for implementing the clock phase selector 131. For instance, if the delay of the total clock path is predictable and within a small range, then a simple fixed value delay line can be implemented for the phase selector. This option has the advantage of being low cost. Alternatively, a coarse phase selector could be used to compare two local pixel clocks, 0 and 180 degrees, and pick the one that provides the best setup and hold time margins for the re-synchronization flip-flops. This method may be preferred for most applications. Yet another alternative is to use a phase-locked-loop (PLL) to develop the correct timing for the resynchronization flip-flops, resulting in the best setup and hold time margins. The PLL could be a simple phase-only tracking circuit. This approach offers finer phase steps than the coarse phase selector.

In the Claims

Please cancel Claim 8.

Please amend Claims 1 and 7 as follows:

1. (Amended) A method for clocking video data to reduce beat patterns, comprising:

receiving a video data signal having a predetermined pixel frequency based on an external clock reference, the video data signal being provided by video data signal circuitry; and

providing a local clock signal to re-clock the video data signal between the video data signal circuitry and output circuitry, the local clock signal being based on the external clock reference, thereby removing interfering influence of other clock signals on the predetermined pixel frequency.

7. (Amended) An integrated video display system for providing a video signal having reduced beat patterns, comprising:

a video data circuit coupled to an output circuit through a latching circuit, the video data circuit being configured to provide a video data signal based on a pixel frequency, the pixel frequency being based on an external clock reference; and

a re-clocking circuit coupled to the latching circuit, the re-clocking circuit being configured to provide a local clock signal for re-clocking the video data signal through the latching circuit, wherein re-clocking the circuit is based on the external clock reference, and the video data signal is provided to the output circuit based on the local clock signal.